Circuit design advances for ultra-low power sensing platforms

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ABSTRACT

This paper explores the recent advances in circuit structures and design methodologies that have enabled ultra-low power sensing platforms and opened up a host of new applications. Central to this theme is the development of Near Threshold Computing (NTC) as a viable design space for low power sensing platforms. In this paradigm, the system's supply voltage is approximately equal to the threshold voltage of its transistors. Operating in this "near-threshold" region provides much of the energy savings previously demonstrated for subthreshold operation while offering more favorable performance and variability characteristics. This makes NTC applicable to a broad range of power-constrained computing segments including energy constrained sensing platforms. This paper explores the barriers to the adoption of NTC and describes current work aimed at overcoming these obstacles in the circuit design space.

Keywords: Ultra-low Power, Sensors, Near Threshold, Voltage Scaling, Energy Efficiency

1. INTRODUCTION

The aggressive miniaturization of CMOS integrated circuits has resulted in a well known dilemma: more transistors can fit on a single chip, but a growing fraction of these devices cannot be used due to power limitations. In high throughput designs, this manifests itself in issues of on-chip temperature variation, packaging reliability, and heat removal. So many devices operating at high speed in such reduced area quickly results in heating and eventual failure. On the other end of the spectrum, in small form factor designs such as sensing platforms, the problem is shifted from heat management to battery lifetime. With advances in circuit and sensor design, pervasive sensor-based systems, from single to thousands of nodes, are quickly becoming a possibility. A single sensor node typically consists of a data processing and storage unit, off-chip communication, sensing elements, and a power source. They are often wirelessly networked and have potential applications in a wide range of industrial domains, from building automation to homeland security to biomedical implants. The versatility of a sensor is directly linked to its form factor – for a sensor to be truly useful in many new application areas, a form factor on the order of $1mm^3$ is desirable while maintaining a lifetime of months or years. To integrate a sensor node with its battery power source in $1mm^3$, energy levels must be reduced by 4-7 orders of magnitude. To achieve this goal, solutions must be developed to deliver the same amount of work using relatively less energy. In other words, the energy efficiency of CMOS circuit implementations must be greatly improved to continue on the path of developing smaller feature-rich systems.

Historically, generations of previous technologies, ranging from vacuum tubes to bipolar to NMOS-based technologies, were replaced by their successors when their energy overheads became prohibitive. However, there is no clear successor technology to CMOS today. The available alternatives are far from being commercially viable, and none has gained sufficient traction, or provided the economic justification for overthrowing the large investments made in the CMOS-based infrastructure. Therefore, there is a strong case supporting the position that solutions to the energy efficiency conundrum must come from enhanced devices, design styles and architectures, rather than a reliance on the promise of radically new technologies becoming commercially viable. In all three of these areas, operating at reduced supply voltages offers the best hope of achieving energy efficiency goals while maintaining acceptable throughput. The question that must be addressed is which voltage reduction scheme should be used and how can its associated design challenges be overcome?

Ultra-low voltage operation, subthreshold in particular ($V_{dd} < V_{th}$), was first proposed over three decades ago to reduce power consumption. However, the various difficulties that arise from operating in this regime have kept subthreshold operation confined to a handful of minor markets, such as wristwatches and hearing aids. To the mainstream designer,

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this range of ultra-low voltage design has remained little more than a fascinating concept with no practical relevance. A more promising variation on this voltage-scaling paradigm is so called "near threshold" operation. By operating CMOS devices at or near their threshold voltage and implementing a host of architectural and circuit techniques, 10× or higher energy efficiency improvements at constant performance can be achieved. This paradigm is referred to as near-threshold computing (NTC) and can be broadly applied to a large range of energy-constrained systems from the highest-end server processors to the smallest sensor platforms.

NTC does not come without some barriers to widespread acceptance, including performance, variation sensitivity, and power management. Sensor-based platforms critically depend on ultra-low power (≤μW in standby) and reduced form-factor (mm^3). Overcoming these barriers in sensor platforms is a formidable challenge requiring a synergistic approach combining methods from the algorithm and architecture levels to circuit and technology levels. Doing so successfully promises to unlock new semiconductor applications, such as implanted monitoring and actuation medical devices, as well as ubiquitous environmental monitoring, e.g., structural sensing within critical infrastructure elements such as bridges.

The rest of this paper is organized as follows. Section 2 provides an overview of the near threshold operating region and discusses the potential benefits of operating in this region. Section 3 details barriers and solutions to NTC system design at the circuit level. Future directions and conclusions are presented in Section 4.

2. NEAR THRESHOLD COMPUTING (NTC)

Energy consumption in modern CMOS circuits largely results from the charging and discharging of internal node capacitances and can be reduced quadratically by lowering the supply voltage (V_{dd}). As such, voltage scaling has become one of the more effective methods to reduce power consumption in commercial parts. It is well known that CMOS circuits function at very low voltages and remain functional even when V_{dd} drops below the threshold voltage (V_{th}). In 1972, Meindl *et al.* derived a theoretical lower limit on V_{dd} for functional operation, which has been approached in very simple test circuits [1]. Since then, there has been interest in systems operated in the subthreshold, initially for analog blocks [2-4] and more recently for digital processors [5-10], demonstrating functionality at V_{dd} below 200mV. In commercial products however, the lower bound on V_{dd} in is still typically set to ~70% of the nominal V_{dd} due to concerns about robustness and performance loss [11-13].

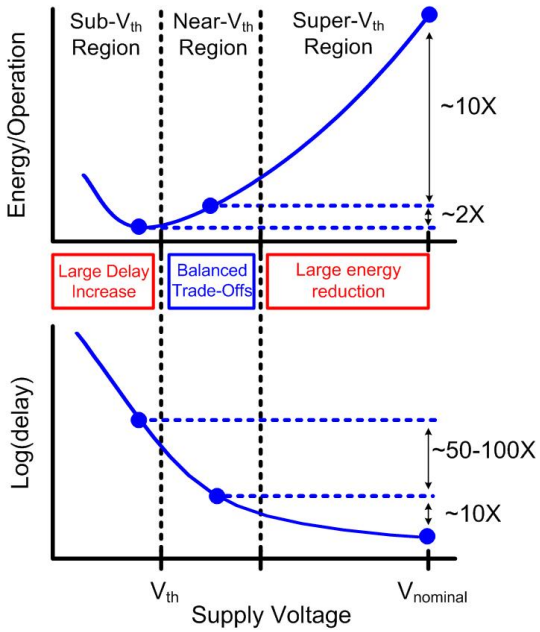

Figure 1: Energy and delay in different supply voltage operating regions.

Given such wide voltage scaling potential, it is important to determine the V_{dd} at which the energy per operation (or instruction) is optimal. In the superthreshold regime, energy is highly sensitive to V_{dd} due to the quadratic scaling of switching energy with V_{dd}. Hence voltage scaling down to the near-threshold regime yields an energy reduction on the order of 10× at the expense of approximately 10× performance degradation, as seen in Figure 1. However, the dependence of energy on V_{dd} becomes more complex as voltage is scaled further below the threshold voltage. In the subthreshold region, circuit delay increases exponentially with V_{dd}, causing leakage energy (the product of leakage current, V_{dd}, and delay) to increase in a near-exponential fashion. This rise in leakage energy eventually dominates any reduction in switching energy, creating an energy minimum.

The identification of an energy minimum supply voltage (referred to as V_{min}, typically in the 250mV - 350mV range) led to interest in processors that operated at this point [9, 10, 14]. This energy minimum however, is relatively shallow. Energy typically reduces by only ~2× when V_{dd} is scaled from the near-threshold regime (400-500mV) to the subthreshold regime, though delay rises by 50-100× over the same region. While acceptable in a few niche applications, this delay penalty is not tolerable for a broader set of applications.

3. NTC DESIGN FOR SENSING PLATFORMS

3.1. Processor Performance

The performance of NTC systems is significantly better than that seen in subthreshold designs and is well suited to sensor platform applications. In an industrial 45 nm technology for example, the fanout-of-four inverter delay (FO4, a commonly used metric for the intrinsic speed of a semiconductor process technology) is only 10X slower at an NTC supply of 400 mV than at the nominal 1.1 V. Given that the performance at nominal supply can achieve clock frequencies in excess of 1 GHz, the reduction imposed by NTC operation is perfectly acceptable in the sensor platform design space. In addition, typical sensing platform operation is heavily duty cycled, with a majority of the system's lifetime being spent in sleep mode. This offers the opportunity to boost the supply voltage for short periods of time in blocks where performance is critical. Workload demands can then be met with little impact on the overall energy requirements.

If we also consider the lowest level of abstraction, performance of NTC systems can be greatly improved through straightforward modifications and optimizations of the transistor structure and its fabrication process. This follows directly from the fact that commercially available CMOS processes are universally tailored to sustaining the super-threshold trends forecasted by Moore's law. In most cases, this results in a transistor that is clearly sub-optimal for low voltage operation. Recently, optimizing for low voltage has generated substantial interest in the academic community because of the potential performance gains that could be obtained by developing a process flow tailored for subthreshold operation. In large part, these gains would be comparable for NTC operation since the devices in question still operate without a strongly inverted channel. For example, Paul *et al.* [15] demonstrate a 44% improvement in subthreshold delay through simple modifications of the channel doping profile of a standard super-threshold device. Essentially, the nominal device is doped with an emphasis on reducing short channel effects at standard supply voltage such as DIBL, punch-through, and V_{th} roll-off. These effects are much less significant when the supply is lowered below about 70% of the nominal. This allows device designers to instead focus on a doping profile that minimizes junction capacitance and subthreshold swing without negatively impacting the device off current.

Entirely new device structures based on fully depleted silicon-on-insulator (FDSOI) technologies are also being considered as candidates for enabling subthreshold applications [16]. The naturally higher subthreshold slope in FDSOI along with its reduced parasitic capacitances make it an attractive option for enhancing performance with little power penalty. Further modifications to the established bulk process methodology, such as using an undoped body with a metal gate structure and removal of the source-drain extensions, serves to improve speed while maintaining standard threshold voltage targets. When these devices are combined using thin-metal interconnect for low-capacitance, the energy-delay product in the subthreshold can be comparable to low power designs operating in the super-threshold. This level of performance makes tailored FDSOI devices highly desirable for NTC design and offers a viable solution for mainstream applications as the process matures.

With similar goals in mind, Hanson *et al*. [17] showed that the slow scaling of gate oxide relative to the channel length yields a 60% reduction in I_{on}/I_{off} between the 90nm and 32nm nodes. This on to off current ratio is a critical measure of stability and noise immunity, and such a reduction results in static noise margin (SNM) degradation of more than 10% between the 90nm and 32nm nodes in a CMOS inverter. As a solution, they have proposed a modified scaling strategy that uses increased channel lengths and reduced doping to improve subthreshold swing. They developed new delay and energy metrics that effectively capture the important effects of device scaling, and used those to drive device optimization. Based on technology computer-aided design (TCAD) simulations they found that noise margins improved by 19% and energy improved by 23% in 32nm subthreshold circuits when applying their modified device scaling strategy. Their proposed strategy also led to tighter control of subthreshold swing and off-current, reducing delay by 18% per generation.

3.2. Coping With Variation

In the near-threshold regime, the dependencies of MOSFET drive current on threshold voltage, supply, and temperature approach exponential. As a result, NTC designs display a dramatic increase in performance uncertainty. Figure 2 shows that performance variation due to global process variation alone increases by approximately 5× from ~30% (1.3×) [18] at nominal operating voltage to as much as 400%, (5×) at 400mV. Operating at this voltage also heightens sensitivity to temperature and supply ripple, each of which can add another factor of 2X to the performance variation resulting in a

total performance uncertainty of 20×. Compared to a total performance uncertainty of ~1.5× at nominal voltage, the increased performance uncertainty of NTC circuits looms as a daunting challenge that has caused most designers to pass over low voltage design entirely. Simply adding margin so that all chips will meet the needed performance specification in the worst-case is effective in nominal voltage design. In NTC design, this approach results in some chips running at $1/10^{th}$ their potential performance, which is wasteful both in performance and in energy due to leakage currents. One potential solution is to employ an architectural approach that dynamically adapts the performance of a design to the intrinsic and environmental conditions of process, voltage, and temperature and tracking these parameters over the wide performance range observed in NTC operation. Such a method is readily complemented by circuit-level techniques for diminishing the variation of NTC circuits and for efficient adaptation of performance. The Razor approach is one recent example [19-21]. A novel flip-flop structure is used to detect and correct for timing errors dynamically. This allows reduction of timing margins via dynamic voltage scaling (DVS) to meet an acceptable error correction rate. While effective, the Razor technique has several inherent difficulties that make it unsuitable for generic sensor platforms, including a complex design cycle and high architectural overhead. As an alternative, performance variation can be tracked an accounted for by measuring critical path timing margins directly. In this way, the architectural overheads can be removed since errors are never allowed to occur in the computation blocks. *In situ* time-to-digital converters are one viable option for implementing such a system and could provide a critical building block to coping with performance variation in NTC circuits [22].

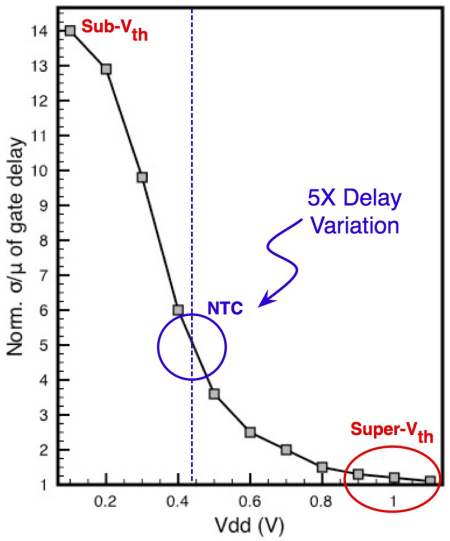

Figure 2: Impact of voltage scaling on gate delay variation.

The increased sensitivity of NTC circuits to variations in process, temperature and voltage not only impacts performance but also circuit functionality. In particular, the mismatch in device strength due to local process variations from such phenomena as random dopant fluctuations (RDF) and line edge roughness (LER) can compromise state holding elements based on positive feedback loops. Mismatch in the loop's elements will cause it to develop a natural inclination for one state over the other, a characteristic that can lead to hard functional failure or soft timing failure. This issue has been most pronounced in SRAM where high yield requirements and the use of aggressively sized devices result in prohibitive sensitivity to local variation.

Several variation scenarios for a standard 6T SRAM cell are shown in Figure 3. In (a), global process variation has resulting in both *P* and *N* type devices being weakened by a V_{th} increase resulting in a potential timing failure during both reads and writes. In (b), the same global effect has introduced skew between the *P* and *N* device strengths. This is particularly detrimental when the *P* is skewed stronger relative to the *N* resulting in a potential inability to write data into the cell. In (c), random local mismatch is considered and the worst case shown for a read upset condition. The cell is effectively skewed to favor one state over another, and the weak pull-down on the left side cannot properly balance the strong access device at its drain. As such, the *Data* node is likely to flip to the "1" state during normal read operations. While these examples are shown in isolation, a fabricated circuit will certainly experience all of them simultaneously to varying degrees across a die and with different sensitivities to changes in supply voltage and temperature. The resulting likelihood of failure is potentially very high, especially as supply voltage is reduced and feature sizes are shrunk.

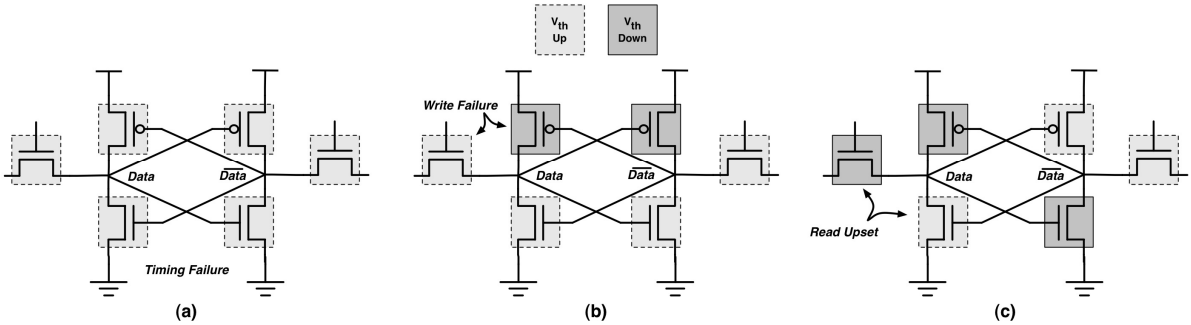

Figure 2 - Effects of global and local variation on a standard 6T SRAM cell. (a) Global Vt reduction resulting in timing failure. (b) Global Vt P-N skew resulting in write failure. (c) Local Vt mismatch resulting in read upset.

For instance, a typical 65nm SRAM cell has a failure probability of ~10^{-7} at nominal voltage, as shown in Figure 4. This low failure rate allows failing cells to be corrected for using parity checks or even swapped using redundant columns after fabrication. However, at an NTC voltage of 400mV, this failure rate increases by ~5 orders of magnitude to approximately 4%. In this case, nearly every row and column will have at least one failing cell, and possibly multiple failures, rendering simple redundancy methods completely ineffective.

The only solution to keeping SRAM viable for NTC applications is to trade-off area for improved low voltage performance. The question then becomes how best to do this – resize and optimize the 6T devices, or abandon the 6T structure completely? One example in which the basic 6T structure was maintained can be seen in the work by Zhai *et al*. [23]. The cell itself is optimized for single-ended read stability, and a supply modulation technique is used on a per column basis to improve writeability. Thus, the read and write operations are effectively decoupled by relying on extra complexity in the periphery of the core array. The result is a cell that is functional below 200 mV and that achieves relatively high energy efficiency.

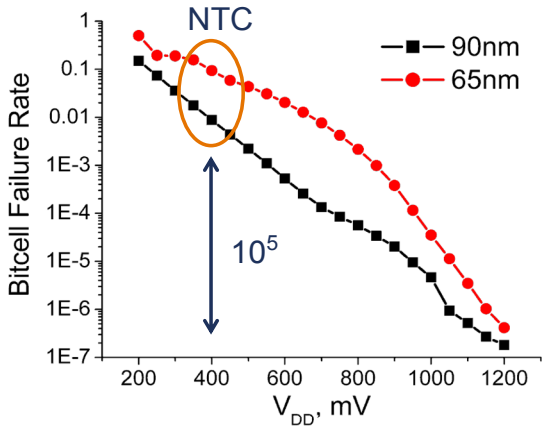

Figure 4: Impact of voltage scaling on SRAM failure rates.

There have also been a number of alternative SRAM cells proposed that are particularly well suited for ultra-low voltage operation. For example, Chang et al. [24] developed an 8T design, in Figure 8, with the premise of decoupling the read and write operations of the 6T cell by adding an isolated read-out buffer, as shown in Figure 5. This effectively allows the designer to optimize the write operation sizing independently of the output buffer and without relying on supply modulation or wordline boosting. This greatly enhances cell stability, but incurs area overhead in the core array to accommodate the extra devices and irregular layout.

Similarly, Calhoun and Chandrakasan [5] developed a 10-transistor (10T) SRAM cell also based on decoupling read and write sizing and operation. The 10T cell is pictured in Figure 5 and offers even better low voltage operation due to the stacking of devices in the read port, though it suffers a commensurate area penalty. Such alternative SRAM cell designs successfully cope with the difficulty of maintaining proper operation at high yield constraints in the subthreshold operating region, and offer promising characteristics for realizing reliable cache in NTC-based systems.

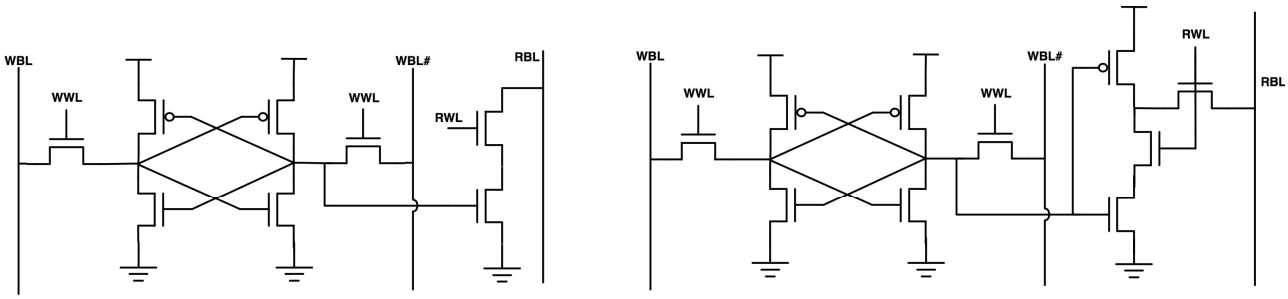

Figure 5: Alternative SRAM Cells: 8T cell [20] and 10T cell [5]

3.3. Power Delivery

Achieving energy efficiency and acceptable processing power at NTC voltage levels leads one to consider exactly how those voltage levels are created. This is an important concern, especially in mobile devices and sensing platforms where power is generally derived from a battery source that has a range of output voltages dictated by applicable chemistries. A typical NTC design will employ a variety of different voltage domains and possibly even necessitate dynamic voltage

levels whose generation is unreasonable to offload outside of the package. Therefore, one can anticipate some level of DC-DC conversion or shunt regulation in every NTC system.

This leads to a critical realization regarding power delivery to NTC circuits: supply regulation in an NTC system must be achieved under strict power budgets to ensure energy efficiency of the overall system. Essentially, the overhead of supply-regulation cannot be allowed to overshadow the gains of NTC voltage scaling. This is particularly difficult to ensure because the circuits responsible for providing high quality supply rails operate from the high voltage level of the power source, and so do not have the luxury of any power reduction through voltage scaling.

Light-load, low-power voltage regulators and converters are beginning to garner attention in recent literature. Low-power control circuitry, novel clocking schemes, and analog circuits with miniscule tail currents are all enabling this transition. For example, a hybrid DC-DC converter and linear regulator system has been reported that can convert from a 3.6V Li-ion battery to subthreshold voltage levels for 5nA to 500nA loads with up to 55% efficiency, representing a 4.6× efficiency improvement over ideal linear regulation [25]. A Fibonacci switched capacitor network (SCN) is used to convert the incoming battery voltage down by a factor of five. Normally, MOS switches in SCNs are large to reduce conductive losses within the network. However, since this SCN network was designed for very low power loads, nearly minimum sized devices are used for switches. This reduces the power overhead required to switch the gate capacitances of these switches and increases the overall efficiency of the system. Typical SCNs are clocked at megahertz levels, but this network uses a 2kHz clock to reduce power overhead. The slow clock is efficiently generated using a specialized timer circuit. To reduce the output ripple when switching so slowly, a linear regulator is used to on the output stage to realize the final supply voltage.

3.4. Conclusion and Future Directions

As Moore's law continues to provide designers with more transistors on a chip, power budgets are beginning to limit the applicability of these additional transistors in conventional CMOS design. This is particularly limiting in sensor type applications where battery capacity is dictated by useful form factor. In this paper we looked back at the feasibility of voltage scaling to reduce energy consumption and extend the usable lifetime of sensing platforms. Although subthreshold operation is well known to provide substantial energy savings it has been relegated to a handful of applications due to the corresponding system performance degradation. We then turned to the concept of Near Threshold Computing (NTC), where the supply voltage is at or near the switching voltage of the transistors. This regime enables energy savings on the order of 10×, with only a 10× degradation in performance, providing a much better energy/performance tradeoff than subthreshold operation. With traditional device scaling no longer providing energy efficiency improvements, our primary conclusion is that the solution to this energy crisis is the universal application of aggressive low voltage operation, namely NTC.

It is clear that the central barriers to NTC processing can be overcome through a variety of device, circuit, and architectural techniques. In addition, power delivery methods for NTC sensor systems are becoming viable due to advances in light load DC-DC conversion even under strict power constraints. However, a pervasive sensing platform solution will require more features than just computation and basic I/O. There is still a broad range of research topics requiring focus in order to enable energy efficiency in analog peripherals and RF components.

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